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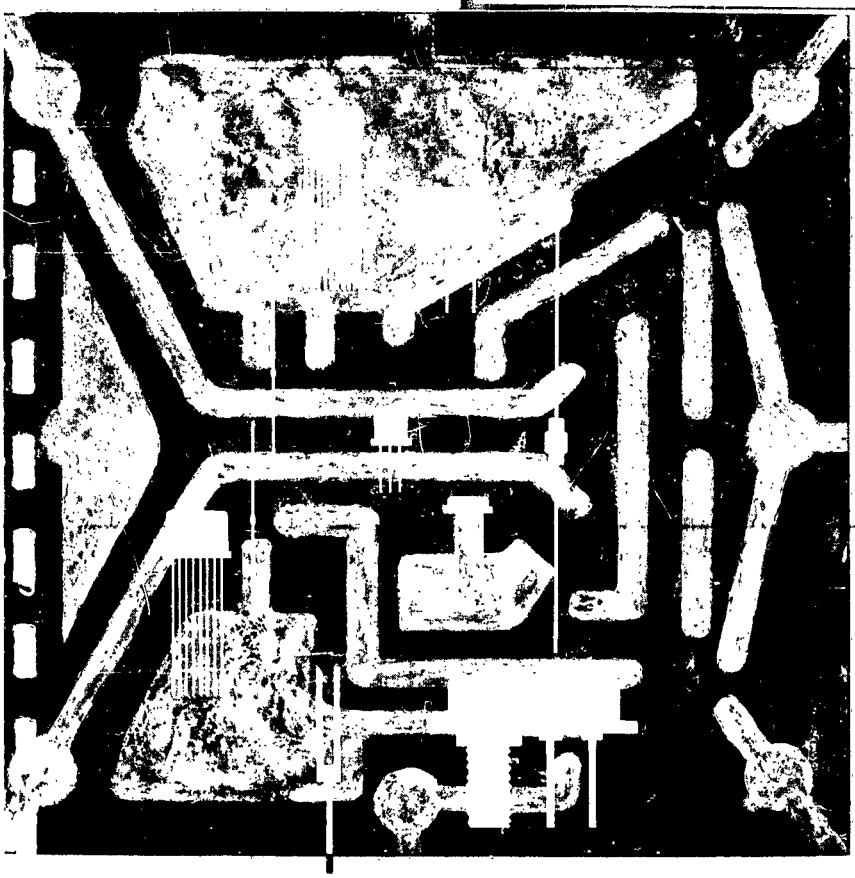

PRODUCTION ENGINEERING MEASURE

Transistor, VHF, Silicon, Power (75W)

SECOND QUARTERLY REPORT

1 October 1962
to
31 December 1962

PSI Report No. 3000:47-Q-2

Prepared By

R. N. Clarke
R. C. Neville
J. W. Ewins

Edited By

B. Rappaport

U.S. Army Electronics Materiel Agency
Contract No. DA 36-039 SC-86733
Order No. 19055-PP-62-81-81

Pacific Semiconductors, Inc.
TRW Electronics
THOMPSON RAMO WOOLDRIDGE INC.

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Research and Development Department
14520 South Aviation Blvd.
Lawndale, (Los Angeles County), California

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Contract No. DA 36-039 SC-86733
Order No. 19055-PP-62-81-81

This contract calls for the establishment of a limited production facility, the delivery of 2,475 25-watt, 100-megacycle transistors, and a study of the requirements for beginning a large scale production operation.

Prepared By

R. N. Clarke, R. C. Neville, J. W. Ewins

Edited By

B. Rappaport

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SECTION I - ABSTRACT

Process improvements, package design and new contacts have been the major areas of activity throughout the second contract quarter. Additional work on test circuitry and beginning material preparation has been initiated. The beryllium oxide tab has been under intensive investigation and considerable knowledge has been gained. Environmental and mechanical testing of the package has been initiated to guide in further packaging changes.

SECTION II - PURPOSE

The terms of the contract require the contractor to establish a limited production facility using prototype equipment capable of producing parts directed toward a rate of 200 transistors, that meet the applicable specifications, per 8-hour shift. During the contract period the contractor shall deliver a total of 2,475 transistors, of which 375 are engineering samples, 100 are pre-production samples, and 2000 are pilot production transistors. The 2000 transistors produced during the pilot run shall meet the applicable technical specifications. The specifications include performance as an amplifier - the transistor must be capable of 25 watts of power output at 100 megacycles with 10 db of power gain - and as an oscillator, the transistor must deliver 25 watts at a frequency of 100 megacycles. In addition, the package must be such that the transistor is electrically isolated from the case.

The prototype equipment required for the establishment of the pilot production run will be developed and supplied at the expense of the contractor.

Upon completion of the pilot production run, a Step II Study will be made to determine the requirements of a manufacturing facility capable of producing 50,000 units per month meeting

the applicable technical specifications and based on one 8-hour shift per day. The necessary plans and schedules required to establish the production capability based upon equipment capacity and pilot production yields shall be incorporated in the Step II Study.

SECTION III - TECHNICAL DISCUSSION

CHAPTER 1

Introduction

The second quarter of PEM Contract No. DA 36-039 SC-86733 has been largely devoted to information gathering. The transistors produced under the Research and Development Contract No. DA 36-039 SC-87342 are capable of operating to the desired specifications. However, with respect to manufacturability, dc characteristics and power amplification performance at assigned frequency (100 MC) considerable performance gains could be realized.

It is realized that the prime motivation behind a PEM contract is to make a given device available to the circuit designer at an earlier period than would otherwise be practical. However, the purpose is defeated if the device produced is so difficult to assemble as to increase its cost prohibitively, if it is used so close to its upper operating limits as to be potentially unreliable. The production model 25W-100MC transistor should be capable of producing its rated power with a reasonable margin of safety and should be available at a cost making its use economically feasible.

To this end there are several obvious changes possible in the device, the processes used in its manufacture and in the overall package. However, before the changes are made a considerable amount of

information is necessary to negate any chance of entering a cul-de-sac during any processing or design changes.

In Chapter 3 of this section the environmental and electrical testing regimen of the contract are briefly discussed. Data on "Group B" tests and in power gain at frequency indicate that the device performance could be improved immensely by altering the package which is acting electrically as a low pass filter for the device. Several alternatives to the current package have been proposed including: light-house tube, coaxial, the PSI micro-power and an epoxy or silicone resin package. Early trials in primitive versions of these package types have tended to prove very successful, but conclusive informative tests have yet to be performed.

A considerable number of devices experienced failure during this period when the beryllium oxide tab parted company with the molybdenum-manganese metallizing. The problem appears to be the lack of knowledge about the behavior of beryllium oxide. Tests have been devised which give promise of detecting faulty parts before good transistors are mounted on them. These tests are currently undergoing a rigid check before final installation into our process line. Any package changes will have to take the beryllium oxide into account and maintain or decrease the current level of thermal resistance while keeping electrical isolation. This area is discussed in greater detail in Paragraph 2.4.

The device itself could undergo several basic changes and these are discussed in Chapter 2 of this section. In essence, increased high frequency and power performance are desired. An extension of the second breakdown locus and reduced sensitivity to loss of drive are also required of the design to increase the device reliability and performance.

Several changes in processing are being contemplated and are discussed in Paragraphs 2.3 and 2.4. Diffusions are under study in an attempt to assure a more even distribution of breakdowns and increased V_{CEO}. Metallizing changes to give quicker and more positive silicon-metallizing have been instituted and data should be available in the next quarter. A variety of surface treatments applied after mount and leadbond operations have been studied and a cleaning process followed by a high temperature baking operation has been chosen as most optimum.

The remainder of this section will describe the problems encountered and solved in manufacturing devices, information gathered in working toward a more reliable device and information needed in the future.

CHAPTER 2

2.1 Introduction

Information gathered from extensive electrical and mechanical testing (see Chapter 3) is available in large quantities. In addition to a series of experiments aimed at improving device and process performance, the mechanical and environmental tests required in the Research and Development contract for this device (see Contract No. DA 36-039 SC-87342) have yielded considerable information. Progress in device design and experiments in the areas of packaging and diffusion are shown below.

In essence the design breaks down into three general areas of endeavor.

A. Theoretical device design. This section deals with a mixture of empirical input and theoretical knowledge to yield better device performance and is described in Paragraph 2.2.

B. The area of process improvement encompasses both diffusion operations and packaging operations. The packaging operations have received the most effort on this front during the second contract interval. The prime reason for this is explained in Paragraph 2.4 of this section. However, diffusion experiments received a good deal of attention and are discussed in Paragraph 2.3.

C. The area of package improvement is under intensive study at present as the devices are at present far superior to the package in which we must place them. The current state of package design is considered in Paragraphs 2.2 and 2.4.

2.2 Device Design

The transistor design for the device to be produced under this contract is an extension of that employed in producing a 25W-100MC device, developed under U.S. Army Electronics Materiel Agency Contract No. DA 36-039 SC-87342.

While the device under consideration satisfied fully the specifications of both contracts the performance is far from optimum. A few of the problems of the device designer are discussed below.

The device h_{fe} (small signal, current gain) is too small to satisfy the terms of the PEM contract. One solution to this problem is to reduce r_b' and thus increase the h_{fe}. To decrease r_b' the designer finds it most convenient to diffuse both emitter and base in less deeply while cutting the base thickness down to increase transport efficiency. A reduction in diffusion depths while maintaining base thickness will improve r_b' and hence h_{fe}. (See Figure 2.2.0a and 2.2.0b.) When this is done experimentally we do indeed have higher h_{fe}, with both power gain and output performance at 100MC much improved.

However, once the device is made more shallow (the emitter and base junction depths are decreased), problems appear in other areas.

Consider, for instance, a device with lapping damage which has been removed on the surface, but still persists in the silicon. (It has been demonstrated that even strains caused by using a four-point probe, with too heavy a pressure setting, are propagated through an entire wafer and can be seen five and more mils away on the opposite side of a wafer.) This damage will cause variations in the diffusion constants for the diffusants (boron and phosphorous) and the resultant impurity diffusion front will have irregularities. The ideal diffusion front is a straight line (corresponding to a sphere of infinite radius) and any departure from this configuration will result in lower junction breakdowns and in higher leakages. If this damage comes from the "upper" surface the emitter junction will be the most effected and such electronic parameters as V_{CES}, V_{CEO} and V_{EB} will be affected to a greater extent than V_{CBO}. In these cases where damage originates from the collector contact processing (a poor diffusion etc.) the base junction will be more greatly affected causing V_{CBO} to be more affected than V_{EBO}.

Consider again, what happens when a dust spot or small speck of unremoved oxide sits on top of a wafer and a diffusion is then performed. If this speck is in place prior to a base diffusion the result is a cusp in the base diffusion front. The result will be

low V_{CBO} immediately. If the cusp is underneath a planar emitter diffusion the emitter and collector regions may be shorted or the characteristics of the device so grossly affected as to make it useless. If this dirt speck is in place before the emitter diffusion, it is possible to short out the emitter base junction or obtain the floating base characteristic of Figure 2.2.1. As demonstrated in Figure 2.2.2 the deeper the diffusion the less a particle of given size on the surface is likely to effect device performance.

For shallow, highly doped regions additional problems are present. One, often neglected, is the resultant strain in the silicon lattice from the high concentration of impurity in the emitter and base diffusions. The highly strained lattice will produce junctions with leakages which are orders of magnitude higher than would otherwise be expected. Additional effects which alter sintering and alloying behavior during metallizing operations can also be seen.

Thus, the device designer is bound in his efforts to make a shallower device by the current status of technology - by lapping techniques, diffusion methods, photoresist tolerances, grain size of photographic materials and purity of solvents. Only by radical change in device design approach or in state-of-the-art technology can progress to any significant degree be made.

In the somewhat nebulous area of package and device interaction little work has been done until recently by semiconductor manufacturers. However, in view of the extreme powers and frequencies at which the device of interest is asked to operate, this hitherto little understood area has been under attack at PSI.

Considerable evidence is available to convince even the most hardened sceptic of the necessity of considering both package and device simultaneously: 1) The input to any semiconductor PN junction device is clearly capacitive. However, the input to a 25W-100MC device at 100MC in the commer emitter mode is inductive. It is quite obvious then that between the outside of the package and the P-N junction (emitter-base) there exists sufficient inductance to overcome the basic P-N junction capacitance. 2) A large number of devices have been lost when the beryllium oxide-metallizing interface gave away on the electrically insulating beryllia tab. Once the phases had separated, thermal run-away commenced and the devices burned out in a matter of micro-seconds. 3) The problems encountered with faulty metallizing on the parts between the device and the outside world (see Chapter 3, Paragraph 3.1) have severely limited performance by increasing power losses within the package.

The above problems can of course be blamed on the package - and it is clear that the present package design is not optimum for operation at 100MC. It is then the responsibility of the designer to redesign the device and package for each other.

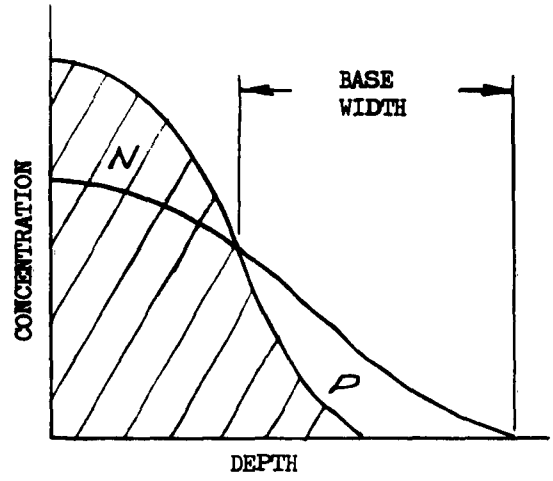


FIGURE 2.2.0.a

DEEP DIFFUSED DEVICE
HIGH r_b'

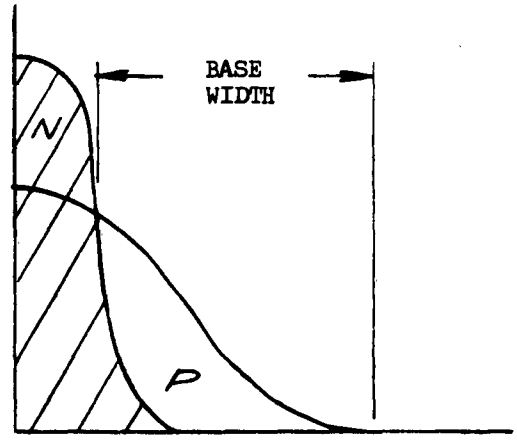


FIGURE 2.2.0 b

SHALLOW DIFFUSED DEVICE
LOW r_b'

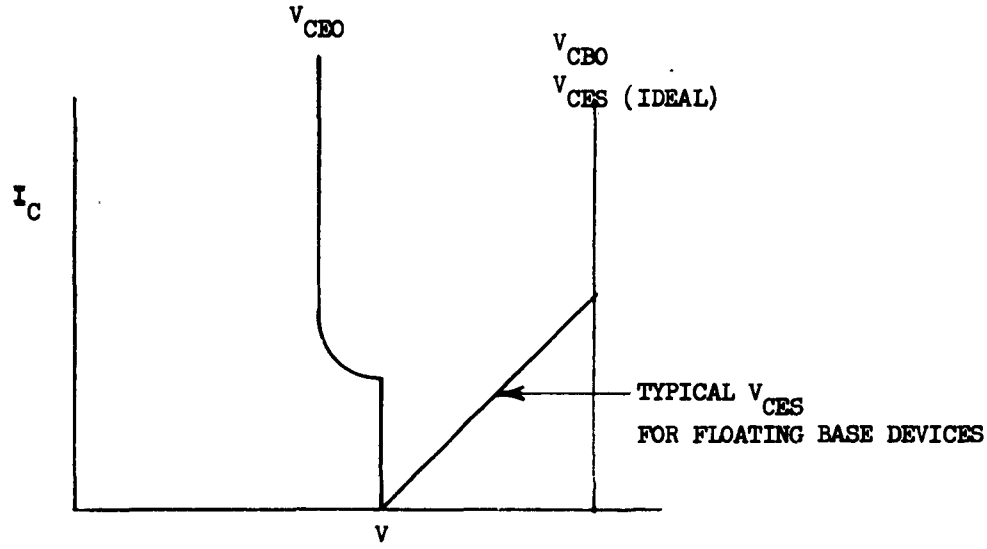


FIGURE 2.2.1
FLOATING BASE CHARACTERISTIC

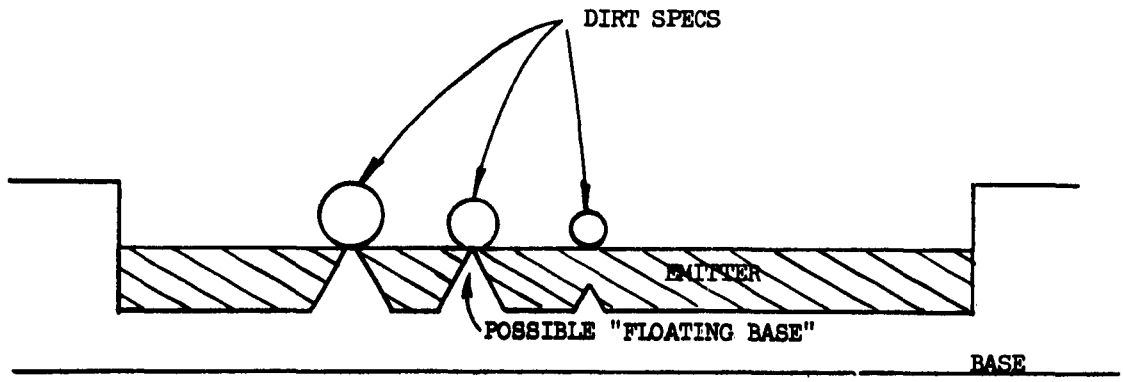


FIGURE 2.2.2

PARTICLE EFFECT ON EMITTER DIFFUSION FRONT

These are some of the problems which we face in an attempt to design the device for better performance, higher reliability and easier manufacture. During the third quarter the redesign of the 75W-PEM transistor will be accomplished in light of the above problems and in view of that which has been learned during the Research and Development Contract No. DA 36-039 SC-87342 and the first two quarters of the PEM contract.

2.3 Diffusion Processes

The state of epitaxial material continues to be reviewed, and these materials will be introduced into the process at such time as they yield leakages and other characteristics comparable to diffused wafers. Collector contact diffusion is being examined at this time with a view to producing consistently lower leakages. In this case lower temperature diffusions are being performed and a continuous diffusion process is being investigated in lieu of the present pre-deposition and redistribution technique. The latter technique had been tried on the variable capacitor diode contract with the Signal Corps (No. DA 36-039 SC-85942), but it was only when the process was returned to a continuous diffusion with the phosphorus glass intact during the entire run, that consistently low leakages were obtained. The results of this work will be reported at a later date. Other sources of phosphorus are also under investigation at the present time with no definitive information yet available.

The area of providing and maintaining a suitable mask oxide for the planar process remains an area of continual investigation. The work here is concerned with the growth of compact and stable oxides in a reasonably short time. An alternate investigation is to find a method to grow a less compact oxide more rapidly, and then compact the oxide in a later process. Experience in this area has reduced the incidence of masking defects; yet it remains as one of the major yield problems.

A serious problem has developed in the diffusion area as a result of the h_{fe} requirement. Prior to this time, the transistor had relatively good yields to all but the h_{fe} specification. Investigations revealed that the h_{fe} could be improved to a point above the specification level by reducing the emitter diffusion depth. Both the base and emitter diffusion depths were reduced accordingly in order to attain the same range of h_{fe} as in the specification by reducing r'_b. The problem which then arose was an incidence of high I_{CES} leakage at these shallower diffusion depths. The I_{CES} problem is definitely junction depth sensitive, being present at junction depths above some dimension. Present work is being directed toward understanding the nature of the problem as well as the possibility of optimizing the junction depth at a point which avoids both problems as a simple immediate expediency. The possible causes being investigated are incomplete diffusions, active areas which are strained or cracked, and the possibility that we are too close to the surface to be able to bond to the active area without affecting the junction. This work is presently being carried out

in a series of experiments designed to establish the actual mechanism. The results of these experiments will be reported at a later date.

2.4 Packaging Processing

This section follows a general outline which can be given as follows:

1. Beryllium Oxide and Brazing
2. Capping and High Frequency
3. Wafer Dicing Processes
4. Crystal Mounting
5. Leadbonding Operations
6. Surface Protection and Its Effects

The two problem areas, electrical isolation and high frequency operation, as outlined in the last quarterly report still represent our major problems in the present package. The situation has been alleviated somewhat, however,as a result of the effort expended during the past period.

The first problem, it will be recalled, is that of achieving complete electrical isolation of the transistor from the case, while maintaining good thermal conductance. Further investigation of materials suitable for this purpose has not disclosed anything superior to beryllium oxide. While beryllium oxide is still a state-of-the-art material, significant advances during the period of this report have been achieved through investigative co-operation between PSI and its suppliers of metallized beryllia.

During the initial investigations of device failures, it was determined that the principle mode responsible for device loss during power dissipation was attributable to failure of the beryllia-to-metallizing bond. Recent evaluations of metallized beryllia have produced semi-quantitative methods of determining the strength of the metallizing-beryllia bond, prior to mounting and power testing transistors. Details as to this test method will be furnished with the Third Quarterly Report. As of this period they are not sufficiently set as to allow publication.

The beryllium oxide or beryllia is metallized first by the application of a molybdenum-manganese mixture, in a suitable vehicle, to the surfaces of the beryllia piece to be metallized. The molybdenum-manganese mixture is then fired into the beryllia, under extremely critical conditions of humidity and temperature. The adherent qualities of the metallizing are further influenced by the structure of the beryllia, and in part determined by the depth of penetration and structure of the molybdenum-manganese. The metallized areas of the beryllia are then plated with a mixture of noble metals for better wetting when brazing to the stud and affixing of the silicon crystal. At present there is some evidence to indicate that, at high temperatures and long periods of time, these metals diffuse through and around the molybdenum-manganese thereby weakening the metallizing-to-beryllium oxide bond. A major effort is being expended to develop a suitable barrier to prevent this possibility, in order to increase device reliability.

Evaluation of beryllia, when received from the supplier, by the above mentioned criteria, (see top of page 15), will prevent or reduce the failures due to poor thermal paths, which will result in higher yields, increased device performance and more economic production.

Brazing techniques (BeO to stud) have been re-evaluated, and as a result, process adjustments and constant process monitoring are providing a good thermal path if properly metallized beryllia tabs are employed. Group B environmental tests (see Chapter 3) show average thermal resistance of properly assembled devices to be 2.2 - 2.3°C/watt with excursions in value between 2.0 - 2.4°C watt.

The second problem, pertaining to the frequency performance of the present package, as noted in a past monthly narrative, is in part a function of materials used in the cap and header pins. These problems originate in:

a. The highly resistive nature of header pins and cap sleeves.
b. The highly resistive plate (nickel and oxides of nickel) on pins and sleeves of the package.
c. The composition of glass used in the glass-to-metal seals of the cap.

Due to the highly resistive nature of header pins and cap sleeves, and considering that, at 100MC, the majority of the current is carried on the conductor surface (skin effect), the high resistance

of the nickel plate and oxides of nickel on the pins and sleeves is highly detrimental to device performance. This detriment was decreased by providing a highly conductive gold plate on the header pins and inner surfaces of cap sleeves and by decreasing the pin and tube lengths (see Figures 2.4.0 and 2.4.1).

The investigation of several new package designs, some with radically new outlines is progressing rapidly. While a completely redesigned package, worthy of the device, is necessary, several interim packages, similar in physical outline to the present package and more closely approaching the qualities necessary for good thermal and high frequency performance are being evaluated.

Modifications to the wafer dicing process which provide a faster rate and more accurate cleavages, thereby minimizing bulk damage and eventually improving device reliability, have been instituted this quarter. Results have been most encouraging showing a 25% increase in dicing yields.

The crystal mounting process and equipment has undergone extensive modification in order to improve rates and yields, and to provide the best possible crystal bonds. The K and S crystal mounting station, previously used, employed a vacuum needle to pick up and position a crystal, deposit it on the beryllia surface and hold the crystal while it is being "scrubbed"* onto the gold silicon solder to remove any contact oxides. Due to the particular annular-like

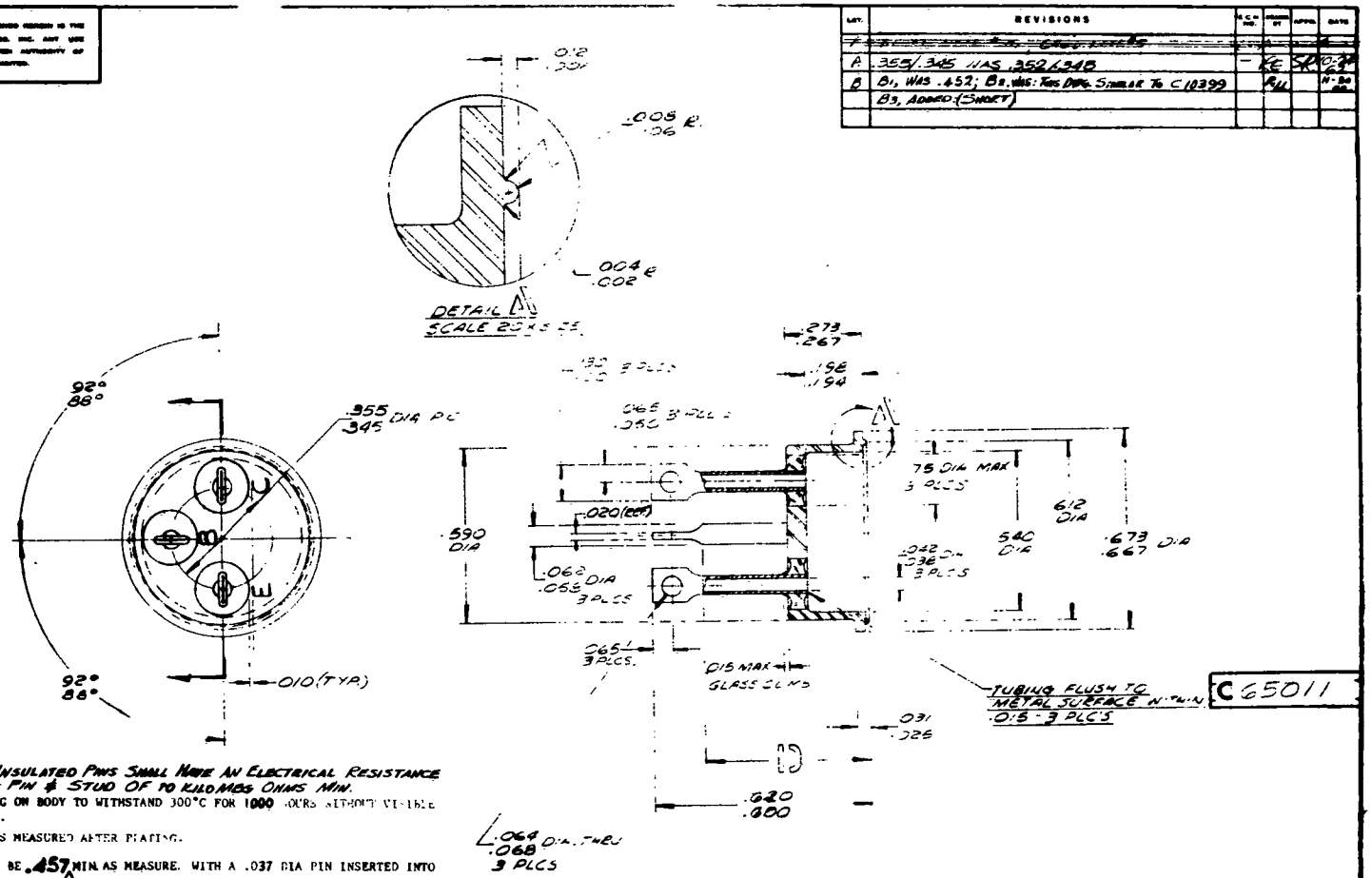
* vibrated rapidly while in intimate contact with the header.

structure of the device the vacuum needle had a tendency to damage the base and emitter metallized stripes if scrubbing was attempted prior to alloying of the silicon with the silicon-gold solder. The crystal is now mounted by hand, held by tweezers, on a stud held in a deep well heating column. The use of a deep well allows a more efficient reducing gas envelope. Employing these mounting stations, higher rates and yields can be effected with less expensive equipment.

The leadbond process was modified to provide a higher rate and correspondingly higher yields by pre-heating of the mounted assembly prior to the actual operation. Fewer "cold" joints are experienced with a resulting increase in satisfactory electrical testing.

Work has continued in an effort to reduce the contributions of device assembly to leakage and to enhance the surface protection provided by the thermally grown oxides of the planar process. To this end modification of present cleaning processes, alternate processes and surface protectants are under investigation. A surface protectant, in current use, that provides surface isolation as well as entrapping residual surface contaminates, appears to be approaching the desired result, but only at some expense to frequency performance. Exactly how much power this process is costing is presently under investigation.

A comprehensive program is under way to completely re-evaluate all processes in order to gain more extensive knowledge concerning their effects upon device characteristics, as a means of more accurately predicting the effects of their variation.



LET.	REVISIONS	E.C.N. NO.	DRAWN BY	APPD.	DATE
A	.355/.345 WAS .352/.348	—	KE	SR	10-27-65
B	B1, WAS .452; B2 WAS: TUBE DIMS. SIMILAR TO C10399		KE		N-30-66
	B3, ADDED (SHEET)				

11.- THE THREE INSULATED PINS SHALL HAVE AN ELECTRICAL RESISTANCE BETWEEN PIN & STUD OF 10 KILOMEG OHMS MIN.

10. NICKEL PLATING ON BODY TO WITHSTAND 300°C FOR 1000 HOURS WITHOUT VISIBLE DETERIORATION.

9. ALL DIMENSIONS MEASURED AFTER PLATING.

8. DEPTH 'D' SHALL BE .457 MIN AS MEASURE. WITH A .037 DIA PIN INSERTED INTO THE TUBE.

7. MELTING POINT OF BRAZE USED MUST BE MORE THAN 500 C.

6. STAMP AS SHOWN LETTERS: E, B & C .06" HIGH. GOTHIC STYLE.

5. LEAK TEST: TEMPERATURE CYCLE 5 TIMES -55°C, 25°C, 100°C, 25°C, AND SO ON, THEN CHECK FOR A LEAK RATE TO BE LESS THAN 5×10^{-8} CC/SEC AS MEASURED BY A HELIUM LEAK DETECTOR UNDER ONE ATMOSPHERE PRESSURE DIFFERENTIAL.

4. TWIST TEST: GLASS MUST WITHSTAND WITHOUT DETERIORATION TO THE SEAL A 20 INCH - OUNCE TORQUE APPLIED 1/4" FROM GLASS.

3. TUBES TO BE HERMETICALLY SEALED & FREE OF FOREIGN IMPURITIES INSIDE. IF BRAZING IS USED FOR SEALING, THERE SHALL BE NO FLUX USED INSIDE THE TUBES. BODY SHALL BE NICKEL PLATED PRIOR TO FIRING. AFTER FIRING THERE SHALL BE NO PLATING OR OTHER CHEMICAL TREATMENT OF PARTS BUT THEY SHALL BE SEALED IN PLASTIC BAGS TO PREVENT FOREIGN MATERIALS FROM ENTERING TUBES.

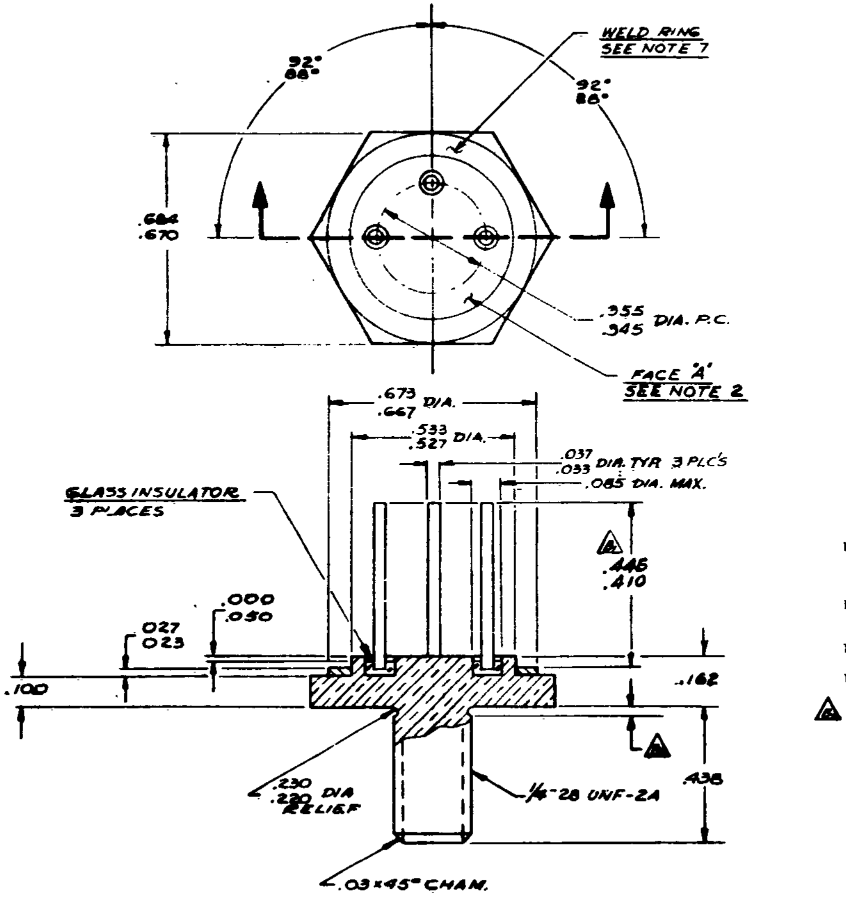
2. MATERIAL: BODY: C. R. S.
INSULATOR: GLASS
TUBE: NICKEL-IRON ALLOY

1. BREAK ALL EDGES AND CORNERS. 010 RAD. MAX.

NOTES:

FIG. 2.4.0 CAP
25 W, .00 MC AMPLIFIER

LTR.	REVISIONS				DATE
A	.355/.345 WAS .352/.340	–			
	B_1 WAS $\frac{.335}{.305}$; B_2 DELETED G.N.#14				
	B_3 DELETED; RELIEF DIM. .210/.220; B_4 ADDED				



NOTES

1. BREAK ALL EDGES AND CORNERS .010 R. MAX.
2. FACE 'A' TO BE FLAT WITHIN ± .001.
3. THE THREE INSULATED PINS SHALL HAVE AN ELECTRICAL RESISTANCE BETWEEN PIN AND STUD OF 10 KILOMEGOHMS MIN.
4. BEARING SURFACE UNDER HEAD TO BE FLAT WITHIN .001 MAX. AND SQUARE WITH THREAD C.L. WITHIN .003 T.I.R.
5. UNIT MUST WITHSTAND BRAZING IN A REDUCING ATMOSPHERE WITH EASY-FLO 45 WITHOUT REMELTING OF BRAZING MATERIAL, CREATION OF VOIDS IN GLASS OR DETERIORATION OF PLATING. PINS SHALL BE SUPPORTED DURING BRAZING OPERATION.
6. NO VOIDS ARE PERMISSIBLE (UNDER 10 POWER MAGNIFICATION) ON BRAZED OR GLASS SURFACE
7. WELD RING TO BE LOW CARBON STEEL. SURFACE INDICATED TO BE FLAT WITHIN .001 T.I.R. AND PARALLEL TO THE UNDERSIDE OF THE HEX, ON THE CIRCUMFERENCE WITHIN .002 T.I.R.
8. COMPLETE THREAD TO EXTEND TO AT LEAST .085 OF HEAD.
9. ALL DIMENSIONS TO BE MET AFTER PLATING WITH .0002 - .0005 DULL NICKEL.
10. UNIT MUST NOT BE DAMAGED BY A 10 IN LB. TORQUE APPLIED TO A FULLY ENGAGED 1/4-28 UNF-2B FULL NUT ASSEMBLED ON THREADS. AFTER APPLICATION OF TORQUE THREADS MUST FIT INTO A "GO" GAUGE.
11. THE USE OF AN EYELET WITH THE GLASS INSULATED PIN IS ACCEPTABLE PROVIDED THE MAX. O.D. DOES NOT EXCEED .085.
12. GLASS AND/OR EYELET NOT TO PROTRUDE ABOVE FACE "A".
13. UNITS TO BE BURR AND CHIP-FREE AND SO PACKAGED FOR SHIPMENT AS TO PREVENT BENT PINS OR DAMAGED THREADS.
14. ~~THIS DRAWING SIMILAR TO C10346~~

C65010

[redacted]

FIG. 2.4.1 STUD BASE
25 W, 100 MC AMPLIFIER

CHAPTER 3

TESTING

3.1 Introduction

A considerable amount of testing has been accomplished during the past period. In particular several modifications were made to optimize the power gain test (see Appendix of First Quarterly Report). These modifications are itemized in the following sections.

In addition to purely electrical testing there exists a class of tests known as environmental and mechanical tests. In general these tests are called "Group B" Tests, and are performed on pilot line samples at the end of any PEM contract. However, it appears profitable to begin Group B tests early on this device. There are several reasons for this and these are enumerated briefly below:

1. The package* is relatively new and requires a thorough check to assure us, the user, of its reliability in mechanical testing.

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* See First Quarterly Report - Contract DA 36-039 SC-86733

2. The use of beryllium oxide tabs places upon the device unusual requirements in the thermal and electrical isolation tests. In light of the problems experienced with the beryllia pieces (see Chapter 2, Paragraph 2.4) it is essential that the behavior of this little understood material be thoroughly investigated.

3. Because the electrical characteristics of the current package are non-optimum (see Chapter 3, Paragraph 3.3) some modifications are desirable. To perform these modifications intelligently the current package should be thoroughly characterized.

3.2 Environmental Testing

The contract requires a number of "Group B" or environmental tests. A quick listing of these tests follows together with a short commentary on the test.

Subgroup I

Physical Dimensions:	The packages are checked in this respect upon receipt in our Lawndale facility.

Subgroup II

Solderability:	In the course of checking electrical behavior, this test is performed (in essence) many times a week.

Temperature Cycling:	The beryllium oxide may be a problem here and is being given additional checks on a lot (of beryllia) bases.
Thermal Shock:	Once again a possible beryllium oxide problem exists and each shipment of beryllia is checked when it is received.
Moisture Resistance:	No tests performed to date. With the use of nickel plated-fully sealed packages no problem is anticipated.

Subgroup III

Shock:	There exists two possible problem areas: 1) beryllia 2) the glass seals on the base, emitter and collector leads. This area is under investigation and is currently being checked by our reliability department.
Constant Acceleration:	This area is being investigated at present. No problems are anticipated with the beryllia.

Vibration, fatigue:	The same problems as are encountered in shock are anticipated here. In addition, continual checks must be made to assure quality of our metal-to-silicon bonding processes.
Vibration, Variable Frequency:	Once again we see the possible problem areas of: 1) beryllia 2) lead seals 3) bonding processes.
Subgroup IV	
Barometric Pressure:	There are no problems anticipated with this test.
High-Temperature Operation:	With a continual updating of processes, it will be necessary to run and rerun this test many times. PSI intends to use this test as a diagnostic tool to aid in improving processes.
Low-Temperature Operation:	This test has not been performed but will be in the near future. However, no problems are anticipated. Devices

have operated satisfactorily at -40°C on tests made during the second quarter of the contract.

Thermal Resistance: This test is highly important in view of the electrical isolation achieved by using a beryllium oxide tab between the silicon chip and the header. On extensive tests run to date no trouble has been encountered.

Salt Spray: The package exterior has been designed for spray resistance and no problem is currently anticipated.

Subgroup V

Tension: The devices are checked periodically for this and no future problem is expected in this area.

Torque: The devices are checked periodically for this and no future problem is expected in this area.

Bending Moment The devices are checked periodically for this and no future problem is expected in this area.

Subgroup VI

Storage Life: Devices are currently in this test at the 400 hour point. This test is considered to be an excellent diagnostic test and will be performed a large number of times during the remaining period of the contract.

Subgroup VII

Operational Life: This test is equivalent to Storage Life in being an excellent diagnostic test. A considerable number of such tests will be performed in the next year and a half.

For a more complete description of the mechanics of such tests the reader is referred to the Appendix of the First Quarterly Report of this contract and to Military Specification MIL-S-19500C.

The considerable number of the tests listed above make excellent tools for evaluation of process improvements and have been used as such by PSI in the past. Such use will be continued on the 75-Watt PEM.

3.3 Electrical Testing

The electrical tests performed in connection with the 25 Watt - 100 Megacycle R and D contract and the 75 Watt PEM contract vary little from the standard tests performed on silicon rf-power devices with two exceptions.

The most troublesome test encountered to date is the power gain test:

Power In	2.5 Watts
V_{CB}	80 Volts dc
I_C	600 mAdc
f	100 mc
Power Out	25 Watts Minimum

The circuit used in this test is discussed in the First Quarterly Report of this contract. Problems have not arisen with the circuit, but rather more with the package and the transistor test jigs.

The major problems encountered are discussed in the following:

1) Test jig misalignment: It has been discovered that the test jig employed in our tests needs continual readjustment to maintain optimum contact pressure between jig and transistor.
2) The circuit itself requires frequent recalibration and retuning to minimize power reflection and maintain optimal feedback.

3) The package is a poor one from the standpoint of electrical performance. The over-all configuration of the package was first developed for a 5W-70MC device (PT-657) and at that level of frequency and power is perfectly satisfactory. However, at 100 MC the package is no longer efficient.

   a) The cap sleeves and header pins (see Figure 3.3.0 and 3.3.1) are made of a resistive material which acts as a poor conductor to bias dc currents and the ac signal.

   b) The plating material for the device is a nickel plate which oxidizes to some extent during crystal mounting and lead bonding operations. The resultant coating of Ni and nickel oxides carries the ac-signal at 100MC (the so-called skin effect is important here), and because of its poor conductivity, a considerable portion of both drive and output power is lost in the pins and sleeves.

   c) The glass used as seals between cap sleeves and the cap body proper has a composition which tends to act as a low pass filter. The resultant loss in output and input power inside the package creates far higher internal dissipation than necessary resulting in device failure due to thermal overloading.

For the present, until such time as a package redesign becomes a reality (see Chapter 2, Paragraph 2.2), little can be done about the first and last problems. However, the serious problem to date, the prime reason for device failure from internal overloading, is the highly resistive Ni-nickel oxide plating on pins and sleeves. Here the solution which has been found most effective is a gold plate on the interior of the cap sleeves. This gold coat becomes the prime conductor for the high frequency signals and provides far superior device performance.

In addition a continuing investigation into test circuitry is being made to determine the exact characteristics of device and the types of circuitry - both test and usage circuitry - best qualified to elicit optimum performance from the device. The current test circuitry in the power gain test is collector grounded which fails to make use of the beryllium oxide tab built into each device. For this it would be desirable to use grounded emitter circuitry on the power gain test. Attempts to fabricate such a circuit are being made.

SECTION IV - SUMMARY AND CONCLUSION

The contractor realizes that the major reason for a PEM contract is to make available devices at an early date. Furthermore, it is desirable that the devices be manufactured by processes capable of high values and high yields. To this end PSI is taking the 25W-100MC device produced under Research and Development Contract No. DA 36-039 SC-87342 and is redesigning portions of the device and the processes for its manufacture.

During the period of interest several processes were examined closely:

A. The use of a beryllium oxide tab created problems when metallizing failures became a common cause of device failure. A test has been devised which will enable PSI to determine the quality of beryllia oxide metallizing prior to mounting good devices. This should appreciably increase our yields.

B. A large amount of data was taken and experiments started using standard acceptance testing and "Group B" tests (see Appendix) to provide data on the characteristics of both package and device. To make any sort of basic changes without understanding where we are at present would be extremely foolish.

C. The final cleaning and capping operations have been under study to provide clues on how these processes affect device reliability and performance.

D. The effect on electrical performance of the package has been studies thoroughly. Paragraph 3.0 of Chapter 3 of Section III details the problems uncovered in this study.

In conclusion it should be pointed out that the device and processes as currently constituted are capable of meeting specifications laid down in the contract. However, it is obvious from the results of our work that improvement can be made and that to fulfill the spirit of our contractual obligation we should make them. Problems in packaging, beryllium oxide and in diffusion have been uncovered and solutions are being formulated.

SECTION V - PROGRAM FOR NEXT INTERVAL

1) Continue package evaluation.

2) Complete preliminary redesign study.

3) Continue new diffusion technique investigation and refine current techniques still further.

4) Finalize beryllium oxide tests and work with suppliers to improve general level of quality.

SECTION VI - PUBLICATIONS, REPORTS, AND CONFERENCES

There were no publications or conferences applicable to this contract during this quarter.

The fourth monthly letter report was submitted 13 November 1963.
The fifth monthly letter report was submitted 10 December 1963.
The sixth monthly letter report was submitted 14 January 1963.

SECTION VII

IDENTIFICATION OF PERSONNEL AND EXPENDITURES

Man-Hour Labor Expenditures

Effort expended by professional employees:

Name	Hours
M. Bloom	8
R. Llata	6
R. C. Neville	181
M. O. Preletz	456
D. H. Treleaven	472
W. M. Wilson	100
TOTAL	1223
Effort expended by technicians	1418.75
TOTAL	2641.75

APPENDIX

TRANSISTOR, SILICON, VHF, POWER (75 WATT) TYPE SigC-2N(X-6)

1. SCOPE

1.1 Scope. - This document covers the detail requirements for silicon, VHF, Power Transistors capable of delivering 25 watts of output power with 10 db of power gain at 100 mc.

1.2 Maximum ratings at 25°C. (See 3.2 herein):

BV_{CBO}	BV_{CES}	BV_{EBO}	I_C	P_C	T_J	T_{stg}
Vdc	Vdc	Vdc	Adc	W	°C	°C
180	180	5	1.5	75 (at: T_C= 25°C)	200	-65 to + 200

2. APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on date of invitation for bias, form a part of this specification to the extent specified herein:

SPECIFICATIONS

MILITARY

MIL-F-14072	Finishes For Ground Signal Equipment
MIL-S-19500	Semiconductor Devices, General Specification For

STANDARDS

MILITARY

MIL-STD-202	Test Methods For Electronic and Electrical Component Parts

DRAWINGS

SIGNAL CORPS

SC-A-46600 Preproduction Sample Approval in Lieu of Requirements in Specifications.

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the procuring agency or as directed by the contracting officer. Both the title and number or symbol should be stipulated when requesting copies.)

3. REQUIREMENTS

3.1 Requirements.- Requirements for the transistors shall be in accordance with Specification MIL-S-19500 and as specified herein.

3.2 Abbreviations and symbols.- The abbreviations and symbols used herein are defined in Specification MIL-S-19500 and as follows:

P_i . . . . . power input

P_o . . . . . .power output

LV_{CES} . . . . . sustaining voltage (collector-to-emitter) base short-circuited

3.3 Design and construction.- The design and construction of the transistors shall be in accordance with applicable requirements of Specification MIL-S-19500.

3.3.1 Transistor case.- The transistor case shall incorporate a stud with a mounting nut and lock washer, physically located at the end of the case opposite the leads, to enable ready mounting of the transistor and dissipating the required power. The transistor case shall be electrically insulated from the collector, emitter, and base.

3.3.2 Operating position. - The transistors shall be capable of proper operation in any position.

3.3.3 Finishing of external metallic surfaces.- The finishing of external metallic surfaces shall be in accordance with requirements in Specification MIL-F-14072 for surface classification Type II, except that the requirements in Specification MIL-F-14072, Section 3, Requirements, covering moisture resistance and finish resistance, and Section 4, Quality Assurance Provisions therein, shall not be applicable. If, due to

special conditions of service or design, a contractor desires to use finishes, materials, or processes other than those specified, such proposal including the reasons therefore shall be submitted to the Contracting Officer for approval. At the discretion of the Contracting Officer, samples and test data may be required to substantiate the suitability of the proposed substitute(s).

3.4 Performance characteristics.- The transistor performance characteristics shall be as specified in Tables I and II herein. (See 6.3 herein.)

3.5 Marking.- The transistors shall be marked in accordance with Specification MIL-S-19500 and as follows. In instances where the diminutive size or lack of suitable surface area on the device would prevent a marking accomplishment readable by the unaided eye, 20/20 vision, at eight inches distance from the device, such marking may be omitted directly on the device. All required marking shall be placed on the unit package.

3.5.1 Type-designation marking.- The transistors shall be marked with the letters "SigC" and the "2N" designation of the device. The "2N" designation of the device shall be "(X-6)" until an identification number conforming to the type designation requirements of Specification MIL-S-19500 has been established.

4. QUALITY ASSURANCE PROVISIONS

4.1 General. - Except as otherwise specified herein, the responsibility for inspection, general procedures for acceptance, classification of inspection, and inspection conditions and methods of test shall be in accordance with Specification MIL-S-19500, Quality Assurance Provisions.

4.2 Preproduction Sample Approval. - The Preproduction Sample approval requirements in Signal Corps Drawing SC-A-46600 hereby replace any Qualification requirements referable to the product covered herein.

4.3 Sampling and acceptance criteria for Acceptance Inspection (see 6.2 herein).- For all tests except Life tests, sampling and acceptance criteria shall be in accordance with 4.3.1 and 4.3.2, respectively, herein for Life tests, sampling and acceptance criteria shall be in accordance with requirements for Method B in Specification MIL-S-19500, Appendix C. The respective LTPD (Lot Tolerance Percent Defective) and Max. Acc. No. (Maximum Acceptance Number) requirements in Tables I and II herein shall govern relative to the details in 4.3.1 and 4.3.2 herein.

4.3.1 Sample Size. - The sample size shall be selected by the manufacturer using Table III herein. The sample size so chosen shall be within the Max. Acc. No. limit associated with the LTPD specified in Tables I and II herein.

4.3.2 Sample acceptance criteria.- For the sample size tested, the Acceptance Number "(a)" in Table III shall not be exceeded. (Rejection number "r" = "(a)" + 1.)

4.4.4 Tightened inspection.- Tightened inspection on resubmitted lots is obtained by testing to an LTPD equal to or less than one-half of the specified initial LTPD.

4.4 Specified LTPD and Max. Acc. No.- The LTPD and Max. Acc. No. specified for a subgroup in Tables I and II herein shall apply for all of the tests, combined, in the subgroup.

4.5 Destructive tests.- The Group B, Subgroups 2, 3, 4, 5, 6, and 7 tests are considered destructive. However, the tests of Subgroups 2, 3, 4, 5, 6, and 7 can be considered non-destructive if sufficient evidence is presented to the Government inspection authority to that effect. Acceptable evidence, for example, would be repeating of all Subgroups 2, 3, 4, 5, 6, and 7 tests, ten times, without significant device degradation. This test repetition procedure need be done only once at inception of Acceptance Inspection, provided that no change in design, or of production techniques, has been effected.

4.6 Disposition of sample units.- Sample units that have been subjected to and have passed Group B, Subgroups 2, 3, 4, 5, 6 and 7 tests not determined to be destructive tests may be delivered on the contract sample units are subjected to and pass Group A inspection. Defective units from any sample group that may have passed group inspection shall not be delivered on the contract or order until the defect(s) has been remedied to the satisfaction of the Government.

4.7 Particular examination and test procedures.-

4.7.1 Sustaining Voltage Test. - The sustaining voltage of the collector with respect to the emitter shall be measured under the conditions specified, with the base short-circuited to the emitter.

4.7.2 Oscillator Power Output Test.- The specified voltage and current shall be applied to the respective terminals under the conditions specified and the power output of the oscillator shall be measured at the frequency specified.

4.7.3 Base Spreading Resistance test.- The specified voltage and current shall be applied to the respective terminals, with the transistor in the common-emitter configuration. An a-c small signal of the high frequency specified shall be applied to the input terminals, and the output terminals shall be short-circuited. The real part of the short-circuit input impedance shall be measured and assumed equal to the base spreading resistance.

4.7.4 Tension test.- The specified force shall be applied to each

lead in the direction of the axis of the lead. The force shall not be applied to more than one lead at a time, and all leads shall be tested.

4.7.5 Torque Test.- The specified torque shall be applied to the stud and about its axis. The stud shall not have become loosened nor the threads damaged, as a result of this test.

4.7.6 Bending Moment test - The transistor shall be mounted by the normal mounting means. The specified force shall be applied, without shock, at right angles to the lead and near the end of the lead.

Table 1. Group A Inspection

MIL-S-19500 Approx. C Ref. Par.	Examination or Test	Conditions	LTPD	Max. Acc. No.	Symbol	Limits Min.	Limits Max.	Unit
	Subgroup I		Major:5 Minor:10	3 4				
30.13	Visual and mechanical Examination	---			---	---	---	---
	Subgroup II		5	3				
50.6	Collector cutoff current	V_{CB} = 180Vdc I_E = 0			I_{CBO}	---	5	mAdc
50.6	Emitter cutoff current	V_{EB} = 5 Vdc I_C = 0			I_{EBO}	---	5	mAdc
50.9	Collector cutoff current	V_{CE} = 180Vdc V_{EB} = 0			I_{CES}	---	5	mAdc
50.9	Collector cutoff current	V_{CE} = 70Vdc V_{EB} = 0			I_{CES}	---	1	mAdc
50.40	Static forward-current Transfer ratio	V_{CE} = 50Vdc I_C = 1.5Adc			h_{FE}	10	---	---
50.40	Static forward-current Transfer ratio	V_{CE} = 70Vdc I_C = 715mAdc			h_{FE}	15	45	---
1/	Sustaining Voltage	I_C = 100mAdc V_{EB} = 0			LV_{CES}	90	---	Vdc
50.25	Saturation Voltage	I_C = 1.5Adc I_B = 300mAdc			$V_{CE(SAT)}$	---	0.75	Vdc

Table 1. Group A Inspection - (Continued)

MIL-S-19500 Appx. C. Ref. Par.	Examination or Test	Conditions	LTPD	Max. Acc. No.	Symbol	Limits Min.	Limits Max.	Unit
	Subgroup 3		5	3				
50.15	Power Gain	V_{CE} = 70Vdc I_C = 715mAdc f = 100mc P_i = 2.5W $T_c \leq 55^oC$ 2/			P_g	10	---	db
3/	Oscillator power output	V_{CE} = 70Vdc I_C = 715mAdc f = 100mc $T_C \leq 55^oC$			P_o	25	---	W
4/	Base Spreading Resistance	V_{CE} = 70Vdc I_C = 715mAdc f = 100mc			r'_b	---	10	ohms
50.19	Output Capacitance	V_{CB} = 70Vdc I_E = 0 f = 1mc			C_{ob}	---	25	µµf
50.33	Small-signal short-circuit forward-current transfer ratio	V_{CE} = 70Vdc I_C = 715mAdc f = 100mc			h_{fe}	7	---	db

1/ See 4.7.1 herein.
2/ Test Circuit as mutually acceptable to Contracting Officer's Technical Representative and contractor.
3/ See 4.7.2 herein. Test circuit as mutually acceptable to Contracting Officer's Technical Representative and contractor
4/ See 4.7.3 herein.

Table II. Group B Inspection

MIL-S-19500 Appx. C Ref. Par.	Examination or Test	Conditions	LTPD	Max. Acc. No.	Symbol	Limits Min.	Limits Max.	Unit
	Subgroup I		10	2				
30.9	Physical dimensions	---						
	Subgroup II		10	3				
40.12	Solderability	---			---	---	---	---
40.14	Temperature Cycling	$T_{(high)}$ = +200°C Test Cond. C 1/			---	---	---	---
40.16	Thermal Shock	$T_{(high)} = 100° \pm 3°C$ $T_{(low)} = 0° \pm 2°C$			---	---	---	---
40.6	Moisture Resistance	No initial conditioning			---	---	---	---
	End-point tests:							
50.9	Collector cutoff current	V_{CE} = 180Vdc V_{EB} = 0			I_{CES}	---	10	mAdc
50.9	Collector cutoff current	V_{CE} = 70Vdc V_{EB} = 0			I_{CES}	---	2	mAdc
50.6	Emitter cutoff current	V_{EB} = 5Vdc I_C = 0			I_{EBO}	---	10	mAdc
50.40	Static forward-current Transfer Ratio	V_{CE} = 70Vdc I_C = 715mAdc			h_{FE}	13	50	---

Table II Group B Inspection - (Continued)

MIL-S-19500 Appx. C. Ref. Par.	Examination or Test	Conditions	LTPD	Max. Acc. No.	Symbol	Limits Min.	Limits Max.	Unit
	Subgroup 3		10	3				
40.10	Shock	Non-operating 5 blows each in each orientation X1, Y1, Y2, Z1 (Total= 20 blows)			---	---	---	---
40.4	Constant acceleration (Centrifuge)	G = 20,000			---	---	---	---
40.18	Vibration, fatigue	V_{CB} = 20Vdc V_{EB} = 5Vdc			---	---	---	---
40.20	Vibration, variable frequency	---			---	---	---	---
	End-point Tests: Same as for Subgroup 2, above							
	Subgroup 4		10	3				
40.1	Barometric pressure (reduced)	Test Cond. B V_C-to-case = 180Vdc V_E-to-case = 180Vdc V_B-to-case = 180Vdc			---	---	---	---
30.6	High-temperature operation	T_A = + 150°C						
50.6	Collector cutoff current	V_{CB} = 70Vdc I_E = 0			I_{CBO}	---	10	mAdc

Table II. Group B Inspection - (continued)

MIL-S-19500 Appx. C. Ref. Par.	Examination or Test	Conditions	LTPD	Max. Acc. No.	Symbol	Limits Min.	Limits Max.	Unit
	Subgroup 4 - Cont'd)							
30.7	Low-temperature operation:	T_A = -55°C						
50.40	Static Forward-Current Transfer Ratio	V_{CE} = 70Vdc I_C = 715mAdc			h_{FE}	8	---	---
30.11	Thermal resistance	---			θ_{J-C}	---	2.33	°C/W
40.9	Salt spray (corrosion)	Test Cond. A			---	---	---	---
	End-point tests: Same as for Subgroup 2, Above							
	Subgroup 5		10	3				
40.15	Tension	Force = 5 lb. 2/			----	----	---	---
40.17	Torque	Torque = 30 in/lb. 3/			---	---	---	---
4/	Bending moment	Force = 1 lb.			---	---	---	---
	Subgroup 6		λ 5	3	---	---	---	---
40.7	Storage Life	Method B $T_{Stg.}$ ≥ +200°C			---	---	---	---
	End-point tests: Same as for Subgroup 2, above							

Table II. Group B Inspection - (Continued)

MIL-S-19500 Appx. C. Ref. Par.	Examination or Test	Conditions	LTPD	Max. Acc. No.	Symbol	Limits Min.	Limits Max.	Units
	Subgroup 7		$\lambda = 5$	3				
40.7	Operation Life	Method B V_{CB} = 20Vdc I_C = 350mA			---	---	---	---
	End-point Tests							
	Same as for Subgroup 2, Above							

1/ + Per Method 102A in Standard MIL-STD-202.

2/ See 4.7.4 herein

3/ See 4.7.5 herein

4/ See 4.7.6 herein.

5. PREPARATION FOR DELIVERY

5.1 Preparation for delivery. - Preparation for delivery shall be in accordance with Specification MIL-S-19500.

6. NOTES

6.1 Notes. - The notes included in Specification MIL-S-19500, except for those covering qualification (see 4.2 herein) and the following, are applicable to this document.

6.2 Ordering data. - If this document is used with the "C" or later issue of Specification MIL-S-19500 containing LTPD-method Acceptance Inspection requirements, the solicitation should indicate that the Acceptance Inspection LTPD-methods requirements in paragraphs 4.3 through 4.3.3 herein shall be considered superseded by the pertinent requirements in the "C" or later issue of Specification MIL-S-19500.

6.3 Establishment of Additional Tests and Parameters.- The resolution of any additional tests and parameters that will serve for optimum performance evaluation of the device relative to the application need is encouraged. It is expected that such determination(s) will be by mutual agreement between the contractor and the responsible Government agency, and will be included in the final acceptance criteria for the device. Pertinent electrical, physical, mechanical, and environmental test coverage in Specification MIL-S-19500 should be considered as a primary guide in this regard.